REMARKS

In the Office Action dated April 24, 2006, the Examiner rejected claims 11-12 and 14-26 under 35 USC 102 as anticipated by Prabhu (US Patent 6,873,024) and rejected claims 11-26 under 35 USC 103 as unpatentable over Prabhu and Onishi (US Patent 5,920,142). The Examiner indicated that claims 1-10 are allowable. In response thereto, the applicants have amended claim 11. Claims 11-26 remain at issue.

The Art Rejection

The Examiner has rejected certain claims as anticipated by Prabhu. The Applicants disagree. Prabhu does not anticipate the claims.

Prabhu is directed to the wafer level packaging of imaging die. In Prabhu, a wafer shaped transparent template 20 as illustrated in Figure 2 is created. The template 20 includes a plurality of die cover regions 22 held together by tie bars 24. Recess regions 26 are defined as the space between the regions 22 and the tie bars 24. See column 3, lines 32-44. Once the template is made, it is aligned and laminated onto a semiconductor wafer. See Figure 3. The template is laminated in one of several ways.

In one embodiment, a bead of resin is deposited around the periphery of the imaging circuitry 16 on the die to form a spacing structure 30. See column 3, lines 64-67 and column 4, lines 1-5, which recites:

> Referring to FIG. 5A, a spacing structure 30 formed on a die 12 of wafer 10 is shown according one embodiment of the present invention. With this embodiment, the spacing structure 30 is formed above the imaging circuitry 16 by dispensing a bead of epoxy resin around the periphery of the imaging circuitry 16.

Figure 5A of Prabhu, provided below, clearly shows the bead of epoxy resin forming the spacing structure 30 formed on the surface of the die 12.

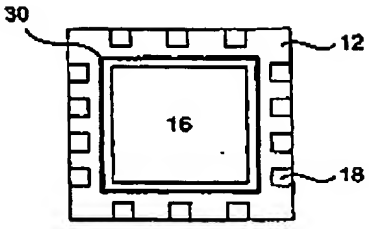

Figure 5A

In an alternative embodiment, a spacing structure 32 is formed by dispensing a layer of clear epoxy over the imaging circuitry 16 on the die. See column 4, lines 18-21, which provide:

> With this embodiment, the spacing structure 32 is formed by dispensing a layer of clear epoxy over the imaging circuitry 16 on the surface of the die 12.

Figure 5B of Prabhu, provided below, clearly shows the layer of epoxy resin 32 forming the spacing structure on the surface of the die 12.

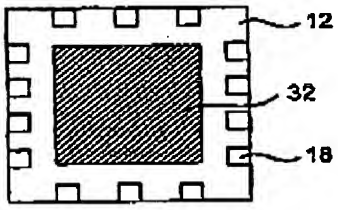

Figure 5B

With either embodiment of Prabhu, the spacing structure is formed on the surface of the die.

In a third embodiment, Prabhu teaches that either the bead of resin or the layer of clear epoxy forming the spacing structure 30 applied onto on the template 20 and then laminated onto the wafer. See column 4, lines 37-39.

Regardless of the embodiment used to mount the template onto the die, Prabhu fails to teach or suggest the use of a **prefabricated** lid having **integral** support regions. Prabhu therefore does not anticipate the claims.

The Examiner has also rejected certain claims as obvious over the combination of Prabhu and Onishi. The Applicants disagree. The Examiner has failed to demonstrate a prima facie case of obviousness because Onishi also fails to teach or suggest the use of a prefabricated lid having integral support regions.

As best illustrated in Figures 1A and 1B, Onishi describes a semiconductor package for a chip (1) having a surface-wave propagation surface (2). The chip (1) is mounted onto a substrate (8). A space retainer (5) is provided for covering and forming a hermetic space 20 over the wave propagation surface (2) of the chip (1). The space retainer (5) includes a support layer (5a) and a cover (5b). The entire package is encapsulated in an epoxy sealing resin (7). See column 10, lines 35-60 and column 12, lines 17-23.

The space retainer (5) of Onishi is <u>not</u> a prefabricated lid having integral support regions. On the contrary, the space retainer (5) is fabricatedin two separate steps. In the initial step, the support layer (5a) is formed on the chip (1) using photolithography. Specifically, column 10, lines 60-67 of Onishi recite:

> The support layer 5a is formed on the chip 1 by conducting exposure by the ordinary exposure method using a photo-mask 111 on a transparent film 111a designed so as to have a partial opening 50 at least at the functional portion 2 and the electrode pads 3 (FIG. 2-b), by conducting development and by carrying out weak alkaline washing, thereby forming the support layer 5a on the chip 1 (FIG. 2-c).

In the second step, the cover (5b) is prepared **separately** using photolithography on a separate film 112a, as illustrated in Figures 2-e through 2-g. Column 11, lines 7-15 of Onishi recite:

> Next, a dry film resist 110 is prepared **separately**. This film resist in its film condition is pattern-formed in the shape of the cover 5b by using a photo-mask 112 on a transparent film 112a designed to cover the opening 50 at the functional portion 2 (FIG. 2-e). The cover 5b is formed on the base film 110a of the dry film resist 110. A base film 113a is held with a frame-shaped clamp jig 113, and an exposure resist 110b having the shape of the cover 5b is transferred onto the support layer 5a by heating under pressure (FIG. 2-g). (emphasis added in bold).

The Onishi reference therefore teaches a two step process for fabricating the space retainer (5). In the first step, the support layer (5a) is fabricated on the chip 1. In the second

step, the cover (5b) is **separately** fabricated on a **separate** transparent film (112a). The Onishi reference therefore fails to teach or suggest the use of a prefabricated lid having integral support regions.

Since neither Prabhu or Onishi, either alone or in combination, fails to teach or suggest the use of a prefabricated lib having integral support regions for mounting onto a die having imaging circuitry, the Examiner has failed to demonstrate a prima facie case of obviousness.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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